

CCD image sensor S9840

High UV sensitivity CCD image sensor



S9840 is a back-thinned type CCD image sensor specifically designed for spectrometers. S9840 has low noise, low dark signal and wide dynamic range. These enable low-light-level detection by setting a long integration time. S9840 has a pixel size of $14 \times 14 \mu\text{m}$ and active area of $28.672 \text{ (H)} \times 0.196 \text{ (V)} \text{ mm}$ (2048×14 pixels).

Features

- Optimized structure for full line binning (1D operation)
- High quantum efficiency in UV region
- Stable UV response
- Low dark current (MPP operation)
- No image-lag

Applications

- Spectrometer, etc.

General ratings

Parameter	Specification
Pixel size	14 (H) × 14 (V) μm
Number of pixels	2080 × 20 pixels
Number of active pixels	2048 × 14 pixels
Active area	28.672 (H) × 0.196 (V) mm
Vertical clock phase	2-phases
Horizontal clock phase	2-phases
Output circuit	Two-stage MOSFET source follower
Package	22-pin ceramic PGA
Window	Quartz glass

Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	Topr	-50	-	+50	°C
Storage temperature	Tstg	-50	-	+70	°C
OD voltage	VOD	-0.5	-	+25	V
RD voltage	VRD	-0.5	-	+18	V
OFD voltage	VOFD	-0.5	-	+18	V
ISH voltage	VISH	-0.5	-	+18	V
IGH voltage	VIGH	-10	-	+15	V
SG voltage	VSG	-10	-	+15	V
OG voltage	VOG	-10	-	+15	V
RG voltage	VRG	-10	-	+15	V
TG voltage	VTG	-10	-	+15	V
Vertical clock voltage	VP1V, VP2V	-10	-	+15	V
Horizontal clock voltage	VP1H, VP2H	-10	-	+15	V

■ Operating conditions (MPP mode, Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	
Output transistor drain voltage	VOD	18	20	22	V	
Reset drain voltage	VRD	11.5	12	12.5	V	
Over flow drain voltage	VOFD	11.5	12	12.5	V	
Output gate voltage	VOG	1	3	5	V	
Substrate voltage	VSS	-	0	-	V	
Test point (input source)	VISH	-	VRD	-	V	
Test point (input gate)	VIGH	-8	0	-	V	
Vertical shift register clock voltage	High	VP1VH, VP2VH	4	6	8	V
	Low	VP1VL, VP2VL	-9	-8	-7	
Horizontal shift register clock voltage	High	VP1HH, VP2HH	4	6	8	V
	Low	VP1HL, VP2HL	-9	-8	-7	
Over flow gate voltage	High	V OFGH	4	6	8	V
	Low	V OFGL	-9	-8	-7	
Summing gate voltage	High	VSGH	4	6	8	V
	Low	V SGL	-9	-8	-7	
Reset gate voltage	High	VRGH	4	6	8	V
	Low	VRGL	-9	-8	-7	
Transfer gate voltage	High	VTGH	4	6	8	V
	Low	VTGL	-9	-8	-7	

■ Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Saturation output voltage	Vsat	-	Fw × Sv	-	V
Full well capacity	Fw	-	130	-	ke ⁻
CCD node sensitivity	Sv	-	4.0	-	μV/e ⁻
Dark current *1	DS	-	40	120	pA/cm ²
Readout noise *2	Nr	-	25	30	e ⁻ rms
Readout speed	fc	-	-	5	MHz
Dynamic range *3	DR	-	5200	-	-
Spectral response range	λ	-	200 to 1100	-	nm
Photo response non-uniformity *4	PRNU	-	±3	±10	%

*1: Dark current nearly doubles for every 5 to 7 °C increase in temperature.

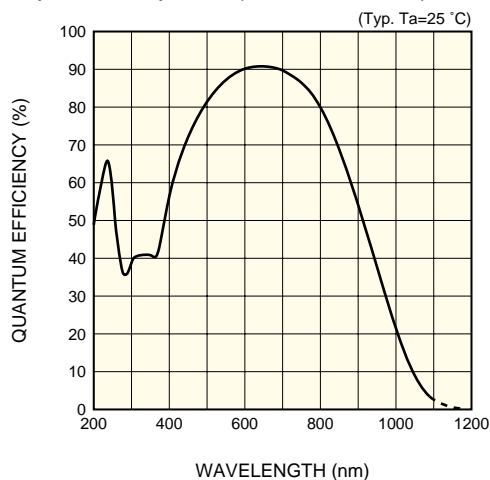
*2: At 2 MHz readout.

*3: Dynamic range (DR) = Full well/Readout noise

*4: Measured at the half of the full well capacity output.

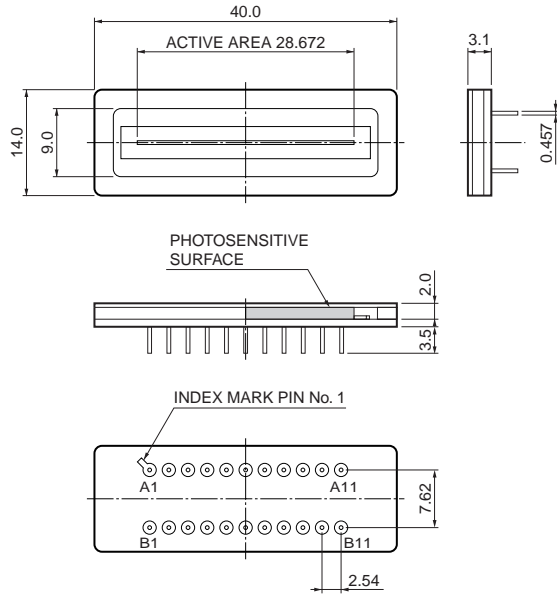
$$PRNU = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100 [\%]$$

■ Spectral response (without window)



KMPDB0247EA

■ Dimensional outline (unit: mm)



KMPDA0186EB

■ Pin connections

Pin No.	Symbol	Function	Remark (standard operation)
A1	OS	Output transistor source, internal RL	Output signal
A2	OD	Output transistor drain	DC (+20 V)
A3	SS	Substrate (GND)	GND
A4	RD	Reset drain	DC (+12 V)
A5	RG	Reset gate	Clock (+6/-8 V)
A6	OG	Output gate	DC (+3 V)
A7	OFD	Output flow drain	DC (+12 V)
A8	OFG	Output flow gate	Same pulse as P1H
A9	P2H	CCD horizontal register clock-2	Clock (+6/-8 V)
A10	P1H	CCD horizontal register clock-1	Clock (+6/-8 V)
A11	ISH	Test point (input source)	DC (+12 V)
B1	SG	Summing gate	Clock (+6/-8 V)
B2	P2V	CCD vertical register clock-2	Clock (+6/-8 V)
B3	P1V	CCD vertical register clock-1	Clock (+6/-8 V)
B4	TG *6	Transfer gate	Clock (+6/-8 V)
B5	-	-	-
B6	-	-	-
B7	RD	Reset drain	DC (+12 V)
B8	SS	Substrate (GND)	GND
B9	P1V	CCD vertical register clock-1	Clock (+6/-8 V)
B10	P2V	CCD vertical register clock-2	Clock (+6/-8 V)
B11	IGH	Test point (input gate)	GND

*6: Isolation gate between vertical register and horizontal register. In standard operation, TG should be applied the same pulse as P2V.